ABSTRACT OF THE DISCLOSURE

By maintaining the gate electrode covered during the process flow for forming metal silicide regions in the drain and source of a field effect transistor, an appropriate metal silicide may be formed on the gate electrode which meets the requirement for aggressive gate length scaling. Preferably, a nickel silicide is formed on the gate electrode, whereas the drain and source regions receive the well-established cobalt disilicide. Additionally, the gate electrode dopant profile is effectively decoupled from the drain and source dopant profile.